A 0.84pJ/cycle Wheatstone Bridge Based CMOS RC Oscillator with Reconfigurable Frequencies

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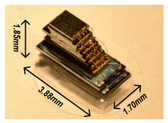
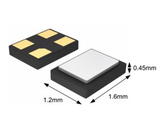
Introduction

Real-Time Clocks (RTCs) are required in low-power IoT devices
- Heavily duty-cycled systems
- Wake up, synchronize, timestamp
- Size, volume, power, cost constraints



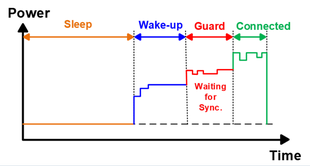
Ref: Q. Dong, et al., ISSCC, 2016



Ref: Abracon LLC, SMD Crystal ABM12

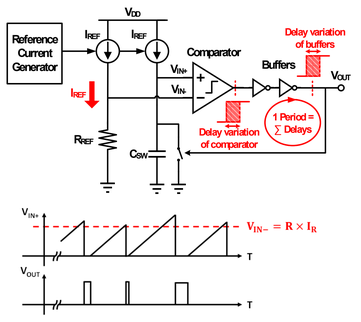
Crystal oscillators
- "Large" volume and footprint

Fully integrated CMOS RC oscillators
Key Metrics: *Energy vs. Frequency stability*



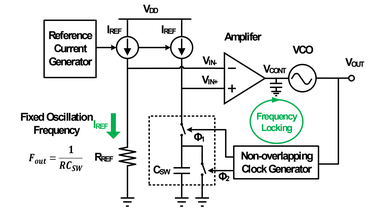
Prior Arts

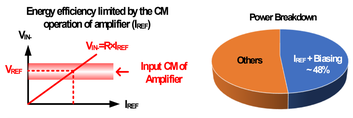
Conventional RC Relaxation Oscillator [1]



Low frequency stability

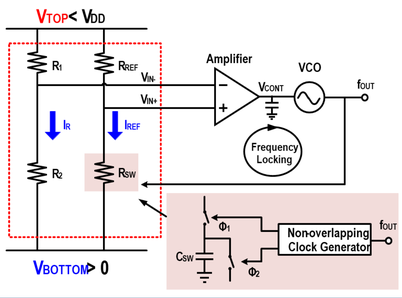
Frequency-Locking Relaxation Oscillator [3]



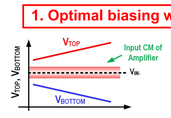


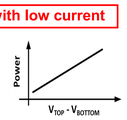
High frequency stability | High power consumption

Proposed Oscillator using Wheatstone Bridge



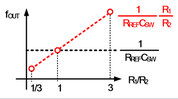
1. Optimal biasing with low current





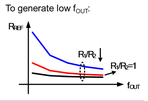
2. Tunable Frequencies

$$f_{OUT} = \frac{1}{R_{REF} C_{SW} R_2}$$



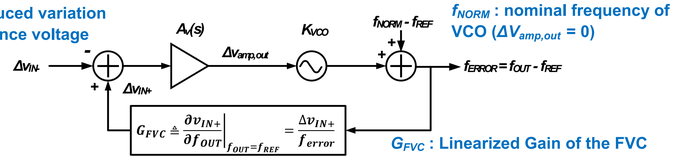
3. Low oscillation frequency with smaller R

$$R_{REF} = \frac{1}{C_{SW} f_{OUT} R_2}$$



Linearized System Modeling

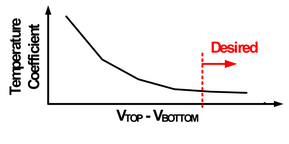
PVT-induced variation of reference voltage

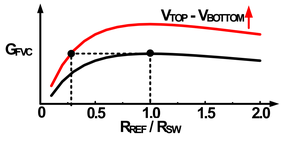


f_{NORM} : nominal frequency of VCO ($\Delta V_{amp,out}$ = 0)

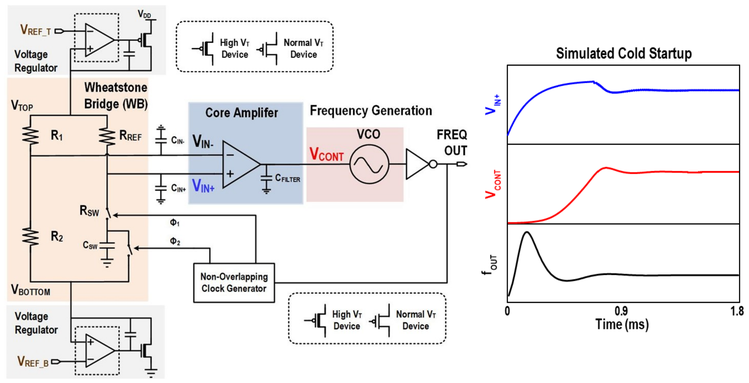
G_{FVC} : Linearized Gain of the FVC

To minimize f_{ERROR}: *1. f_{NORM} should be close to f_{REF}; 2. G_{FVC} should be large enough*



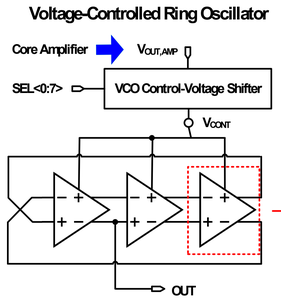


System Implementation

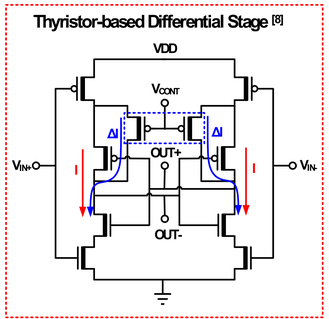


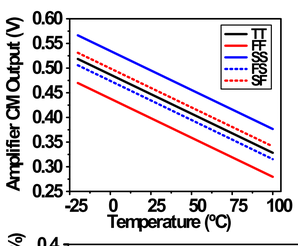
Voltage-Controlled Oscillator

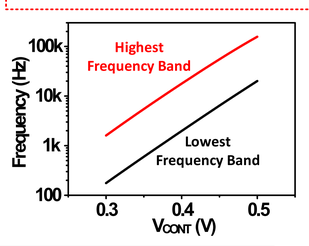
Voltage-Controlled Ring Oscillator

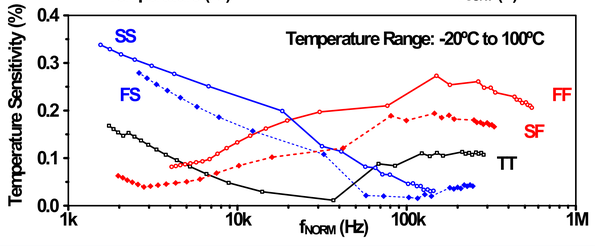


Thyristor-based Differential Stage [8]



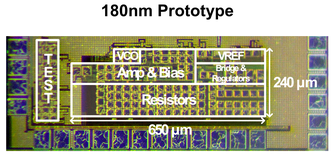


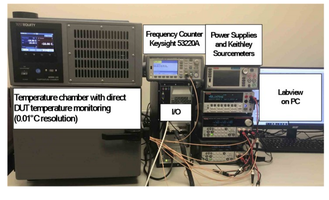




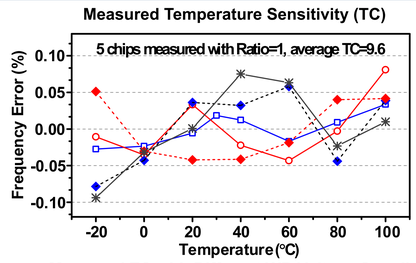
Prototype and Measurement Setup

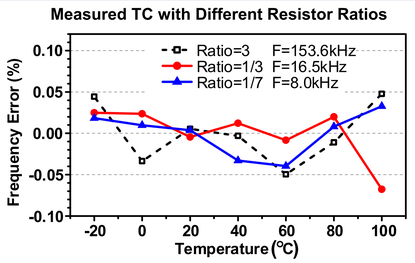
180nm Prototype

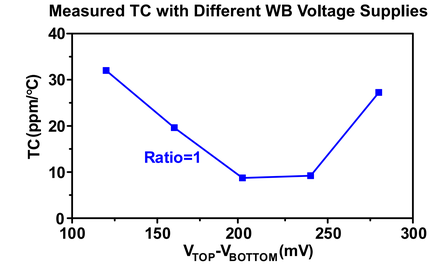


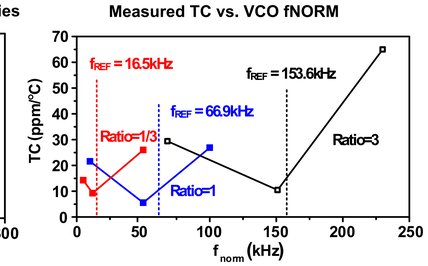


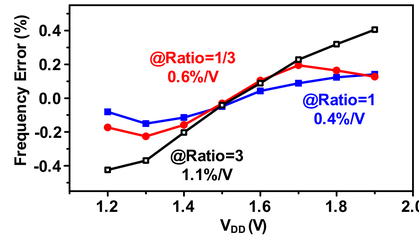
Measurement Results

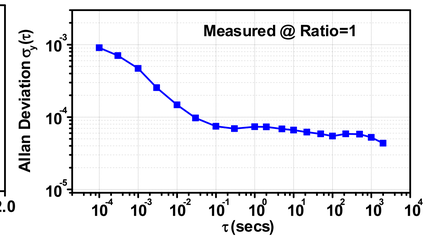








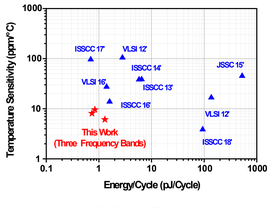




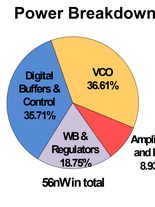
Comparison and Conclusions

	This work			ISSCC '16 [3]	ISSCC '13 [6]	ISSCC '14 [5]	VLSI '12 [7]	JSSC '16 [4]	ISSCC '18 [1]	ISSCC '17 [2]
Technology	180nm			180nm	65nm	65nm	60nm	180nm	180nm	65nm
Frequency (KHz)	66.9	16.5	153.6	3	18.5	32.8	32.8	70.4	7e3	1.35e3
Area (mm2)	0.145			0.506	0.032	0.015	0.048	0.26	1.59	0.005
TC (ppm/°C)	9.6[a]	6.1	8.1	13.8	38.5	38.2[c]	16.7[a]	34.3[a]	3.85[b]	96
Temperature Range (°C)	-20 to 100			-25 to 85	-40 to 90	-20 to 90	-20 to 100	-40 to 80	-45 to 85	0 to 150
Number of Samples	5			1	1	5	4	5	12	2
Line Sensitivity (%/V)	0.4	0.6	1.1	0.49	1	0.09	0.125	0.75	0.18	0.49
Supply Voltage Range (V)	1.2 to 1.9			0.85 to 1.4	1.3 to 3.3	1.15 to 1.45	1.6 to 3.2	1.2 to 3	1.7 to 2	0.9 to 1.9
Power (nW)	56	xx	113	4.7	120	190	4480	110	750	920
Energy/Cycle (pJ/Cycle)	0.84		0.74	1.6	6.5	5.8	136.6	1.56	93.8	0.7

[a] Average value of measured samples [b] Calculated using box method [c] Max value among measured samples.



Power Breakdown



56nW in total

[1] A. Paidimarri, et al., "A 120nW 18.5kHz RC oscillator with comparator offset cancellation for ±0.25% temperature stability," ISSCC 2013.
[2] A. Savanth, et al., "A0.68nW/kHz supply-independent Relaxation Oscillator with ±0.49%/V and 96ppm/°C stability," ISSCC 2017.
[3] D. Griffith, et al., "A 190nW 33kHz RC oscillator with ±0.21% temperature stability and 4ppm long-term stability," ISSCC 2014.
[4] C. Gürleyük, et al., "A CMOS Dual-RC frequency reference with ±250ppm inaccuracy from −45°C to 85°C," ISSCC 2018.
[5] M. Choi, et al., "A 11nW Resistive Frequency Locked On-Chip Oscillator with 34.3 ppm/°C Temperature Stability for System-on-Chip Designs," JSSC, 2016.
[6] T. Jang, et al., "A 4.7nW 13.8ppm/°C self-biased wakeup timer using a switched-resistor scheme," ISSCC 2016.
[7] K. Hsiao, "A 32.4 ppm/°C 3.2-1.6V self-chopped relaxation oscillator with adaptive supply generation," VLSIC 2012.
[8] I. Lee, et al., "A Constant Energy-Per-Cycle Ring Oscillator Over a Wide Frequency Range for Wireless Sensor Nodes," JSSC, 2016.

Conclusions

A Wheatstone Bridge-based CMOS Timer
- Eliminates high biasing power in prior arts
- Supports tunable oscillation frequencies with low area overhead
- VCO's f_{NORM} can track f_{REF} for better temperature stability

180nm CMOS Prototype
- Best-in-class 9.6ppm/°C temperature sensitivity
- 0.84pJ/cycle energy efficiency