
ZHIYU CHEN

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EDUCATION

Ph.D. Candidate in Electrical and Computer Engineering	07/2021-present
Rice University, Houston, TX	GPA: 3.83/4.0
M.S. in Electrical Engineering	08/2018-07/2021
Rice University, Houston, TX	
B.S. in Electrical Engineering	09/2014 -07/2018
Nanjing University, Jiangsu, China	GPA: 87.6/100

PUBLICATIONS

Journal Publications

- A. Pakala, Z. Chen, Y. He, K. Yang, "MBSNTT: A Highly Parallel Digital In-Memory Multi-Bit-Serial Number Theoretic Transform Accelerator for Homomorphic Encryption, " under review.
- Z. Chen, Z. Yu, Y. He, S. Lin, D. Li, J. Wang, Y. Wang and K. Yang, "CAP-RAM: A Charge-Domain In-Memory Computing 6T-SRAM for Accurate and Precision-Programmable CNN Inference," in *IEEE Journal of Solid-State Circuits (JSSC)*, 2021.
- Y. Zhou, Z. Chen, J. Lin and Z. Wang, "A High-Speed Successive-Cancellation Decoder for Polar Codes, " in *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, 2019.

Conference Publications

- *Y. Zhao, *Z. Chen, Q. An, Y. Fu, C. Li, Y. Lin, K. Yang, "ELLA-PIM: Efficient S-PIM Accelerators via Enhancing Data Locality and Lower-bit Activations," under review. (*equal contribution)
- *Q. Jin, *Z. Chen, Y. Wang and K. Yang, "PIM-QAT: Neural Network Quantization for Processing-In-Memory (PIM) Systems," under review. (*equal contribution)
- Z. Yu, W. Wang, J. Chen, Z. Chen, Y. He, A. Singer, J. Robinson, K. Yang, "A Wireless Network of 8.8-mm³ Bio-Implants Featuring Adaptive Magnetoelectric Power and Multi-Access Bidirectional Telemetry," in *Radio Frequency Integrated Circuits Symposium (RFIC)*, 2022. **(Best Paper Finalist)**
- Q. Jin, J. Ren, R. Zhuang, S. Hanumante, Z. Li, Z. Chen, Y. Wang, K. Yang, S. Tulyakov, "F8Net: Fixed-Point 8-bit Only Multiplication for Network Quantization, " in *International Conference on Learning Representations (ICLR)*, 2022. **(Oral)**
- Z. Chen, Q. Jin, Z. Yu, Y. Wang, K. Yang, "DCT-RAM: A Driver-Free Process-In-Memory 8T SRAM Macro with Multi-Bit Charge-Domain Computation and Time-Domain Quantization," in *Custom Integrated Circuits Conference (CICC)*, 2022.
- *Y. Huang, *Z. Chen, D. Li, K. Yang, "CAMA: Energy and Memory Efficient Automata Processing in Content-Addressable Memories," in *International Symposium on High-Performance Computer Architecture (HPCA)*, 2022. (*equal contribution)
- Z. Chen, Q. Jin, J. Wang, Y. Wang, K. Yang, "MC²-RAM: An In-8T-SRAM Computing Macro Featuring Multi-Bit Charge-Domain Computing and ADC-Reduction Weight Encoding," in *International Symposium on Low Power Electronics and Design (ISLPED)*, 2021.

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- Z. Li, G. Yuan, W. Niu, Y. Li, P. Zhao, Y. Cai, X. Shen, Z. Zhan, Z. Kong, Q. Jin, Z. Chen, S. Liu, K. Yang, B. Ren, Y. Wang and X. Lin, "NPAS: A Compiler-aware Framework of Unified Network Pruning and Architecture Search for Beyond Real-Time Mobile Acceleration," in *Conference on Computer Vision and Pattern Recognition (CVPR)*, 2021.
 - Z. Chen, J. Lin and Z. Wang, "Reduced Complexity List Polar Decoder with an Improved Path Pruning Scheme," in *International Conference on Communications Technology (ICCT)*, 2017. **(Best Presenter Award)**

Patents

- K. Yang and Z. Chen, "Training Method for Neural Network for Processing-In-Memory Systems," U.S. Provisional Application No. 63/221249, filed July 2021.
- K. Yang and Z. Chen, "Charge-Domain In-Memory Computing Circuits," U.S. Patent No. 17761116, filed March 2022.
- Z. Chen, J. Lin and Z. Wang, "An Improved Path Pruning Scheme Based on List Successive-Cancellation Decoding of Polar Codes," CN Patent No. 107666325 B, issued July 2021.

RESEARCH

Mixed-Signal Machine Learning Accelerators

08/2018-present

Advisor: Prof. Kaiyuan Yang, Rice University

- Designed and fabricated a compact, accurate and programmable in-memory computing (IMC) 6T-SRAM macro for CNN inference
- Designed and fabricated a high compute-density and high energy efficiency IMC 8T-SRAM macro for CNN inference
- Co-designed and evaluated IMC architectures for end-to-end CNN inference
- Developed IMC-aware CNN training quantization framework to minimize accuracy loss due to non-idealities in IMC

Automata Processing Accelerators

06/2021-present

Advisor: Prof. Kaiyuan Yang, Rice University

- Design an area- and energy-efficient automata processing accelerator using content-addressable memories (CAM)

High Performance Polar Decoders

09/2016-06/2018

Advisor: Prof. Zhongfeng Wang, Nanjing University

- Designed a low-complexity and hardware-friendly decoding algorithm for polar codes
- Designed approximate computing units for high-throughput polar decoders

PROFESSIONAL EXPERIENCE

Aizip Inc, Saratoga, CA

05/2022-08/2022

- Position: Circuit and Architecture Design Intern
- Responsibility: 1. Provide technical support for the Charge-Domain PIM IP; 2. Develop architecture simulator for PIM based AI chip

Apple Inc, Cupertino, CA

06/2021-08/2021

- Position: Digital Circuit Design Intern
- Responsibility: High-speed SRAM design and optimization

AWARDS

Best Paper Finalist, RFIC 2022	06/2022
Rice Graduate Fellowship	08/2018
Outstanding Graduate Thesis in Nanjing University	05/2018
Best Presenter, ICCT 2017	10/2017
Merit Scholarship, Nanjing University	10/2016
Merit Scholarship, Nanjing University	10/2015

TEACHING

- **ELEC 423: Digital Integrated Circuits Design**
Teaching Assistant, Rice University, Spring 2022
- **ELEC 521: Advanced Digital Integrated Circuits**
Teaching Assistant, Rice University, Fall 2021
- **ELEC 423: Digital Integrated Circuits**
Teaching Assistant, Rice University, Spring 2021
- **ELEC 521: Advanced Digital Integrated Circuits Design**
Teaching Assistant, Rice University, Fall 2020

COURSES & TOOLS

Advanced Integrated Circuits Design (Virtuoso/HSPICE/Perl)
Advanced VLSI Design (Simulink/Vivado HLS)
Analog Integrated Circuits Design (Virtuoso)
Wireless Integrated Circuits (ADS)
Computer Systems Architecture (C/C++)
Deep Machine Learning (Python/Pytorch/Tensorflow)
Embedded Machine Learning (Python/Pytorch/Verilog)
Learning from Sensor Data
R for Data Science (R)
Introduction to Microfabrication

ACADEMIC SERVICE

Journal/Conference Review

- IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)