YAN HE

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CURRENT RESEARCH FOCUS

Low Power ASIC Design, Digital and Mixed-signal Circuits, Hardware Security, Power Management, Clocking, Digital PLL

EDUCATION

Rice University *Aug. 2018 - Sept. 2023 (expected)*
Doctor of Philosophy
Department of Electrical and Computer Engineering

Zhejiang University *Sept. 2014 - Jun. 2018*
Bachelor of Science
Department of Electronic Science and Technology

INDUSTRY EXPERIENCE

Research Intern at Circuit Research Group (CRG), NVIDIA, USA *Mar. 2021 - Jul. 2021*
Manager: Tom Gray, NVIDIA
Mentor: Sduhir Kudva, NVIDIA

- **A stable Physicall Unclonable Function (PUF)**
  - Propose and design a stable PUF circuit using TSMC 5nm FinFET technology. The PUF passed the temperature and voltage stability requirements in post-layout simulation.

ACADEMIA EXPERIENCE

Research Assistant at Rice University *Sep. 2018 - Present*
Advisor: Kaiyuan Yang, Rice University

- **A Fully Synthesizable 100Mbps Edge-Chasing True Random Number Generator**
  - Design and implement a Fully Synthesizable True Random Number Generator (TRNG) based on edge chasing in evenstage ring oscillators (RO). The proposed configurable RO with an automatic self-calibration loop enables robust highspeed operations and high-quality outputs under -40 to 125°C and 0.7 to 1.2V conditions, digital layout mismatch and process variations, and power injection attacks.
  - Ten 65nm prototypes designed in unmodified digital flow using only foundry standard cells demonstrate random bit generation at up to 100.8Mbps and pass all NIST tests without post-processing.
- **A Lossless and Modeling Attack-Resistant Strong PUF**
  - Design and implement a Strong PUF based on a complex network with embedded entropy sources (ES). ES are stabilized by Automated Entropy Source Stabilization (AESS) using in-situ healing or fixing without losing any challenge-response pairs (CRPs) or exposing raw ES values to off-chip.
  - The 65nm prototype achieves <4E-8 BER, consumes 4.28pJ/bit, and operates at 150/540 Mb/s in normal/frequency boost modes. The generated CRPs are resistant to prevalent black-box machine-learning and custom white-box attacks.
- **An ultra-low BER PUF with Automatic Self-Checking and Healing (ASCH) system**

- Design and implement low power and area Physically Unclonable Function (PUF) array and reduce its Bit Error Rate (BER) through efficient and effective cell reconfiguration and masking using ASCH.
- The 65nm prototype achieves a low pessimistic BER of <3E-8, which is limited by the number of measurements.

- **PUF-Controlled Transmitter for Physical-Layer Identification**
  - Design a PUF to control the input bias of a Power Amplifier (PA), changing the output spectrum of the transmitter to enable physical-layer identification. And to counter the effect of PA's transfer function, simulate and implement ROM to flatten the output distribution in the spectrum of interest. Tapeout and measurement were done in GF 45nm.
- **A side-channel attack resistant digital LDO achieving state-of-the-art voltage regulation performance**
  - Design a digital-LDO with an asynchronous and nonlinear ADC (Edge-Chasing Quantizer, ECQ) for side-channel resistance and fast voltage regulation, and a second-path boosting circuit for fast droop recovery. LFSRs are used for additional randomization.
  - The 65nm prototype achieves state-of-the-art regulation performance and more than 14000× improvement in power SCA resistance on a 128b AES engine with negligible design overhead.

Research Intern at University of Michigan *Jul. 2017 - Nov. 2017*
Advisor: Michael P. Flynn, University of Michigan

- **A 2-beam 8-element digital-to-RF beam-forming transmitter**
  - Complete the testing process, including PCB designing, FPGA programming, signal recording and data processing

PUBLICATION

1. **Y. He**, K. Yang, "A Fully Synthesizable 100Mbps Edge-Chasing True Random Number Generator" in IEEE Symposium on VLSI Circuits (VLSI), 2023 (accepted).

2. **Y. He**, D. Li, Z. Yu, K. Yang, "ASCH-PUF: A "Zero" Bit Error Rate CMOS Physically Unclonable Function With Dual-Mode Low-Cost Stabilization" in IEEE Journal of Solid-State Circuits (JSSC), Jan. 2023.

3. W. Li*, **Y. He***, K. Yang, N. Guru, "Scaling electrical percolation networks based on renormalization group theory". Applied Physics A, 128(8), 1-6, 2022. (* indicates equal contributions)

4. Z. Yu, W. Wang, J. C. Chen, Z. Chen, **Y. He**, et al, "A Wireless Network of 8.8-mm^3 Bio-Implants Featuring Adaptive Magnetoelectric Power and Multi-Access Bidirectional Telemetry". IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2022

5. **Y. He**, Q. Yu, K. Yang, "A Lossless and Modeling Attack-Resistant Strong PUF with < 4E-8 Bit Error Rate". IEEE Custom Integrated Circuits Conference (CICC), 2022

6. Z. Yu, J. C. Chen, **Y. He**, et al, " Magnetoelectric Bio-Implants Powered and Programmed by a Single Transmitter for Coordinated Multisite Stimulation," in IEEE Journal of Solid-State Circuits (JSSC), vol. 57, no. 3, pp. 818-830, Dec 2021

7. D. Li, **Y. He**, A. R. Pakala and K. Yang, "MePLER: A 20.6-pJ Side-Channel-Aware In-Memory CDT Sampler," in IEEE Symposium on VLSI Circuits (VLSI), 2021

8. Z. Chen, Z. Yu, Q. Jin, **Y. He**, et al, "CAP-RAM: A Charge-Domain In-Memory Computing 6T-SRAM for Accurate and Precision-Programmable CNN Inference," in IEEE Journal of Solid-State Circuits (JSSC), vol. 56, no. 6, pp. 1924-1935, June 2021

9. Z. Yu, J. C. Chen, **Y. He**, et al, "Multisite Bio-stimulating Implants Magnetoelectrically Powered and Individually Programmed by A Single Transmitter". IEEE Custom Integrated Circuits Conference (CICC), 2021.

10. **Y. He**, D. Li, Z. Yu and K. Yang, "An Automatic Self-Checking and Healing Physically Unclonable Function (PUF) with < 3E-8 Bit Error Rate", IEEE International Solid-State Circuits Conference (ISSCC), 2021.

11. Q. Zhou*, **Y. He*** K. Yang and T. Chi, "Exploring PUF-Controlled PA Spectral Regrowth for Physical-Layer Identification of IoT Nodes," IEEE International Solid-State Circuits Conference (ISSCC), 2021. (* indicates equal contributions)

12. Z. Yu, J. C. Chen, F. T. Alrashdan, B. W. Avants, **Y. He**, et al, "MagNI: A Magnetoelectrically Powered and Controlled Wireless Neurostimulating Implant," in IEEE Transactions on Biomedical Circuits and Systems, vol. 14, no. 6, pp. 1241-1252, Dec. 2020

13. **Y. He** and K. Yang, "A 65nm Edge-Chasing Quantizer-Based Digital LDO Featuring 4.58ps-FoM and Side-Channel-Attack Resistance," IEEE International Solid-State Circuits Conference (ISSCC) pp. 384-386, 2020.

14. Z. Yu, J. C. Chen, B. W. Avant, **Y. He**, et al, "An 8.2mm^3 Implantable Neurostimulator with Magnetoelectric Power and Data Transfer," IEEE International Solid- State Circuits Conference (ISSCC) pp. 510-512, 2020.

15. B. Zheng, L. Jie, J. Bell, **Y. He** and M. P. Flynn, "A Two-Beam Eight-Element Direct Digital Beamforming RF Modulator in 40-nm CMOS," IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 7, pp. 2569-2579, Jul. 2019.

16. B. Zheng, J. Bell, **Y. He**, L. Jie and M. P. Flynn " A 0.19 mm^2 128 mW 0.8-1.2 GHz 2-beam 8-element digital direct to RF beamforming transmitter in 40 nm CMOS " IEEE Radio Frequency Integrated Circuits Symposium (RFIC) pp. 128-131 Jun. 2018.

SELECTED AWARDS

- **Solid-State Circuit Society (SSCS) Predocotral Achievement Award for 2021-2022** *Jan 2022*
- **Best Paper Award at 2021 Custom Integrated Circuits Conference (CICC)** *May 2021*
- **Second-Class Scholarship for Outstanding Merits** *Nov. 2017*
  Award for Top 5% Students Annually, Zhejiang University
- **First-Class Scholarship for Outstanding Merits** *Nov. 2016*
  Award for Top 1% Students Annually, Zhejiang University
- **Second-Class Scholarship for Outstanding Merits** *Nov. 2015*
  Award for Top 5% Students Annually, Zhejiang University

SKILLS AND TOOLS

- **Skills:** Low Power VLSI Circuits Design and Measurement, Verilog RTL simulation, Synthesis, Placement & Routing
- **Software:** Virtuoso, VCS, Design Compiler, Innovus, Calibre, ADS, Hyperlynx, Hspice, Matlab
- **Programming Language:** Python, C/C++, Labview, Perl