Haotian Dai

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Education

- **Rice University** — Houston, TX
  PhD Student, Electrical and Computer Engineering — *Jan 2022 - Present*
- **University of Rochester** — Rochester, NY
  Master of Electrical and Computer Engineering — *Aug 2019 - Dec 2021*
- **Nanjing University** — Nanjing, Jiangsu, China
  Bachelor of Microelectronic Science and Engineering; GPA: 87.8/100 — *Sept 2015 - June 2019*

Coursework

- **Graduate Level**: Advanced Analog CMOS, RF And Microwave Integrated Circuit, Intro to VLSI, Detection Estimation Theory, Nanoelectronic Devices, Intro to Hardware Security
- **Undergraduate Level**: Analog Circuits, Digital Circuits, Circuit Analysis, Audio Electronics, Signal and Systems, Digital Signal Processing, Fundamentals of IC design, Semiconductor Physics, Fundamentals of Semiconductor Devices, Probability and Random Process

Skills

- **Programming**: Verilog HDL, Python (numpy, pandas), MATLAB, Latex, C
- **Platforms**: Cadence Virtuoso, HSPICE, LTSPICE, ASITIC, ADS, Multisim, Linux, Jupyter Notebook, Office
- **Languages**: Mandarin Chinese (Native), English (Proficient)

Research Interest

- Power Management, Hardware Security

Research Experience

- **Distributed DLDO featuring Power Regulation and Secure Hardware Masking**
  Rice University — ***Jun 2021 - present***
  - A novel edge-chasing quantizer (ECQ)-based digital LDO (DLDO) is distributed on local points of power grid to improve both power regulation and validity of independence between masking shares.
  - A simulink model of distributed digital DLDO is establisheds to conduct simulation.
  - Improvement in hardware masking with application of distributed DLDO is analyzed and compared to the cases with single DLDO and without DLDO.
- **Vulnerability of Hardware Masking in Practical Implementations**
  University of Rochester — ***Nov 2020 - April 2021***
  - The dependence between leakage of shares are quantitatively analyzed and a mathematical expression is derived considering parasitic impedance of power delivery network during hardware implementation of masking.
  - Implications of different design parameters of the power delivery network that affect the correlation between the leakage of different shares are explored.
  - Design guidelines to reduce the correlation between the leakage of different shares are discussed with reference to the mathematical expression.
- **Transformation of Student's T-test to Success Rate in Masking Scheme**
  University of Rochester — ***July 2020 - Nov 2020***
  - A transformation of Students's t-test to success rate is analyzed under masking scheme, revealing attack's successful rate based on t-values.
  - A close-form equation is derived to show the relation between t-test and success rate and provide a more concrete evaluation on the security of masking implementation.
- **A Novel Construction of 2D High-performance Artificial Synapse**
  Nanjing University — ***Nov 2018 - May 2019***

- Due to the high proton conductivity of Chitosan and ferroelectric polarization of PVDF-TrFe, a novel artificial synapse is proposed with a sandwich structured FET composed by Chitosan, PVDF-TrFe and C8-BTBT to extend the retention time.
- Chitosan is first spin-coated as a flat substrate, and PVDF-TrFe and C8-BTBT are deposited by coffee-ring-driven assembly successively.
- The proposed synapse shows quick response when being charged and the maintenance time is three times longer compared to the case without PVDF-TrFe.

Publications

- **Dai, Haotian**, and Selçuk Köse. "On the vulnerability of hardware masking in practical implementations." Proceedings of the 2021 on Great Lakes Symposium on VLSI. 2021.
- Chengdong Yang, Jun Qian, Qijing Wang, Sai Jiang, Yiwei Duan, Hengyuan Wang, **Haotian Dai**, Yun Li. "Additive-assisted "metal-wire-gap" process for N-type two-dimensional organic crystalline films," Organic Electronics, 2019, 68: 176-181. [paper link]

Course Projects

- **RF Receiver Front-End Design**
  Team Project ***May 2020***
  - In this project, the front-end of an RF receiver for satellite comm downlink at S-band (2.2-2/3 GHz) is designed with ADS. An LNA, a mixer, seceral filters are implemented in the receiver. The output signal of the receiver frond-end is the intermediate-frequency (IF) signal, which will be converted to digital signals and further processed in the baseband for demodulation and decoding.
- **2-stage OTA Design**
  Personal Project ***Dec 2019***
  - In this project, a low-noise 2-stage OTA for the switched- capacitor type amplifier is designed to be used as a readout for MEMS capacitive accelerometer sensor. The OTA is designed with Cadence Virtuoso to meet a list of specifications.
- **Switched-capacitor Sample & Hold Circuits**
  Personal Project ***Nov 2019***
  - In this project, two sample & hold circuits are designed with Cadence Virsuoto to be capable of sampling input signals with maximum amplitude of 1V and frequencies up to 15 Mhz. The sample-and-hold stages are supposed to be used as an input-stage of a 16-bit A/D converter.
- **Implementation of Logic Module with Verilog HDL**
  Personal Project ***May 2019***
  - In this project, several logic modules are implemented with Verilog HDL on Multisim including Arithmetic logic unit(ALU), Sequence Controller, Counter, Memory and Multiplexer(MUX).
- **Intelligent Car Based on Embedded System**
  Personal Project ***Jan 2019***
  - In this project, an intelligent car is designed to be capable of avoiding obstacle, self-tracing and measuring distance. Python are used on Raspberry Pi to control several types of sensors and realize different functionalities.

Teaching Experience

- **Teaching Assistant for ECE 210 Circuit For Nonmajors**
  University of Rochester ***Fall 2019***
  - Corrected homework, midterm and finals for students, and provided reasons for each single deduction of points.
  - Gave recitation to the students and helped answer their questions with inspiration.
- **Teaching Assistant for ECE 222 Integrated Circuits: Design & Analysis**
  University of Rochester ***Spring 2020***
  - Solved and Corrected homework, quiz and lab project, and provided detailed reasons for point deduction
  - Provided weekly office hour and lab hour for students to address their questions.
- **Teaching Assistant for ECE 429 Audio Electronics**
  University of Rochester ***Fall 2021***
  - Solved and corrected homework and lab reports, and provided detailed reasons for point deduction
  - Held office hours and helped answer students' questions with inspiration.